Call for Papers / Invitation to Special Session

Reconfigurable Embedded Systems (RES)

Special Session co-Chairs:

Alexander A. Barkalov University of Zielona Góra <u>A.Barkalov@iie.uz.zgora.pl</u>

Marek Węgrzyn

University of Zielona Góra M.Wegrzyn@iie.uz.zgora.pl

Digital embedded systems require real-time operations and concurrent processing. Reconfigurable systems are fast, flexible dedicated devices, less power consumable, and can be implemented in programmable logic environment, such as FPGA and CPLD. Users can adjust their systems for particular requirements due to tuning combinational or registered logic functions of the system. In addition, systems can be reconfigurable using methods of partial or even dynamic reconfiguration. As an example, Reconfigurable Application Specific Logic Controllers (ASLC) can be shown.

One of the very important tasks in embedded system design is implementation of its control unit. It can implemented using different models. It is necessary to optimize both hardware resources and/or performance of control unit to improve the corresponding characteristics of resulted embedded system.

Hardware Description Languages (HDL), like VHDL, Verilog or SystemVerilog, are very universal platform for design of embedded systems. A discrete HDL model of Logic Controller, which is derived from the control interpreted Petri net (PN) or microprogram control unit (MCU), is implemented as a FPGA-based control unit, which is nested inside a discrete control system. As synthesis tools become more advanced and user friendly, the entry point in the design process is moving towards higher levels of specification. The design process is greatly simplified due to using FPGA and CPLD compilers.

Submission of Papers

Papers are to be submitted electronically (in PDF) via conference web pages (select as track SS-RES).

Author's Schedule

Deadline for submission of papers: Notification of paper acceptance: Final manuscript: June 14, 2009 July 5, 2009 July 25, 2009

www.desdes.uz.zgora.pl